Weakened Cell Modeling and Simulation

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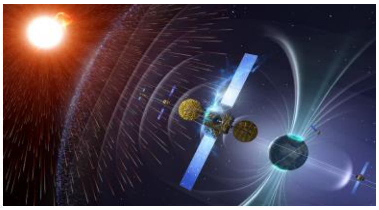
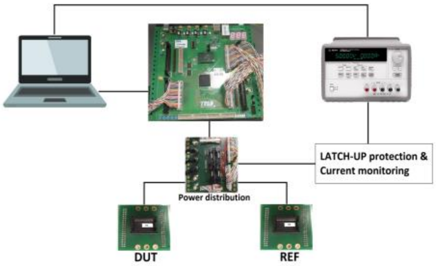
Introduction

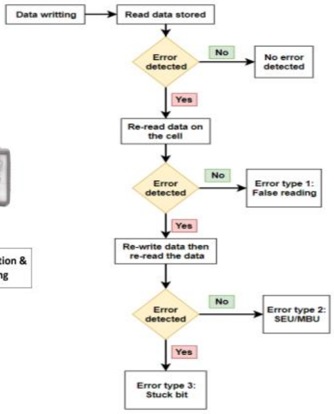
The space environment is full of radiation emitted from the Sun, trapped within Earth's magnetosphere or come from outer Universe. These charge particles are a major cause of satellite anomalies and malfunction on various components. Among those, SDRAM onboard CNES satellites has been degraded and lead to loss of functionality not only under heavy ions but also with other light particles such as protons and neutrons. The failures showed to appear on certain bit addresses causing stuck bits, which may randomly recover and may be stuck again after a period of time, are strongly suggested by displacement damage cluster induced by single particle. In another hand, the leakage current in DRAM cells is an ongoing as it affects directly the refresh rate and leads to an increased power consumption, reducing the lifetime of DRAM cells. Objectives of this PhD are studying from ground based experiment and simulation with TCAD simulator to investigate the basic mechanisms involved.

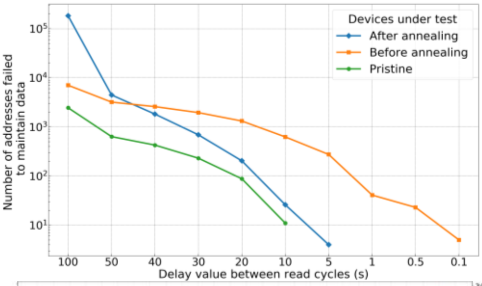


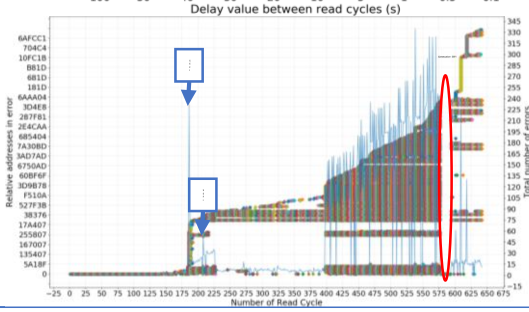
Experimental

In order to understand more in detail the phenomenon, the experiments have been carried on to create these failures on SDRAM at ground level under proton and heavy ion beam.





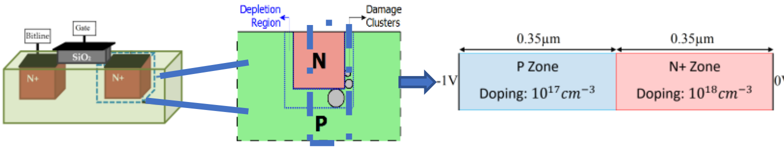


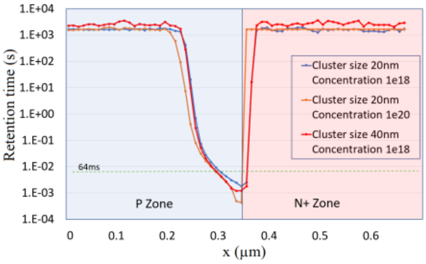


The results showed the retention time degradation under both proton and heavy Ion. At room temperature, devices anneal briefly in a short period of time, anneal using at high temperature recovery device faster. Moreover, the Intermittency behavior is observed on DDR3 DRAM devices under proton and heavy ion. Weakened cell and Intermittent Stuck Bit behavior are caused by leaky mechanism but not stuck at fault type.

Simulation

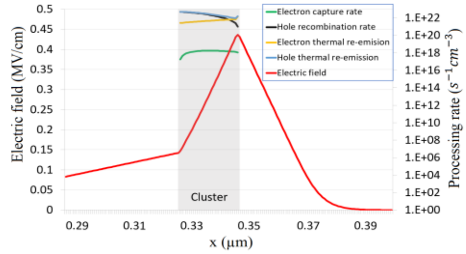
ECORCE (Etude du COmportement sous Radiation des Composants Electroniques) has been used to simulate the device with implementation of damage cluster. ECORCE is based on finite volume method and provides the Multiple Trapping Detrapping (MTD) model which is of particular interest for this study.





Cluster Size	20-100 nm
Cluster Concentration	10^{18}- 10^{20} cm^{-3}
Defect energy level	0.56 eV

As the proof of concept, 1D simulation of the P-N+ junction at the storage node. In this study, we used Gossick model for the cluster of defect. The proposed model for displacement damage cluster is a uniform spherical shape.



The simulations show leakage current increases dramatically when the displacement cluster is within the depletion area. The retention time can drop below the JEDEC standard for refresh rate of DRAM memory.

The width of depletion region is the key parameter to evaluate the sensitive zone which drive by the doping profile and applied voltage. Size downscaling across technology nodes will increase the doping concentrations which will decrease the depletion zone width but increase the cluster-induced junction leakage current.

Conclusion and perspective

Through the experiments, the weakened cells has been observed clearly on DRAM devices. Various factors can be causing the intermittency behavior one of those has been studied by TCAD simulation showed the critical position of damage cluster inside the junction node of the memory cell. The key parameter to evaluate the cell's sensitivity to degradation is the depletion region width, which depends on doping values and storage node voltage applied which will be more important among the aggressive down scaling of technology node.
However, the works still continue with more experiments and simulation in 2D model to further study more possibilities that affect the cell's degradation.