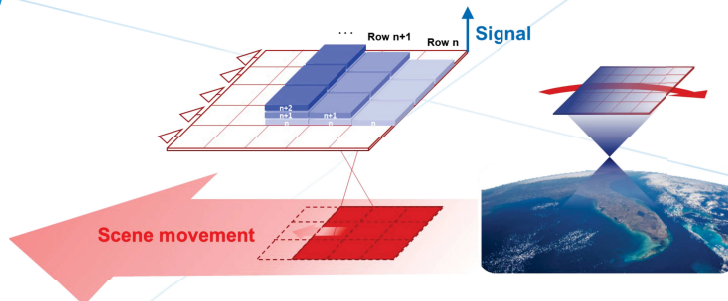


HIGH PERFORMANCE BACKSIDE PIXELS IN CHARGE DOMAIN

Antoine Salih Ali^{1,2,3}, François Roy⁴, Stéphane Demiguel³, Cédric Vimontois², Julien Michelot⁵, Pierre Magnan⁴ and Vincent Goiffon⁴

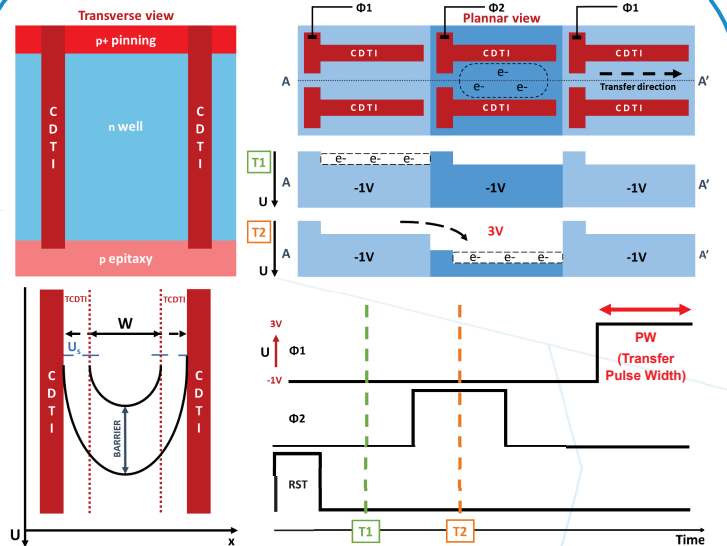
¹ISAE SUPAERO, Toulouse, France. ²Centre National d'Etudes Spatiales (CNES), Toulouse, France.
³Thales Alenia Space, Cannes, France. ⁴STMicroelectronics, Crolles, France. ⁵Pyxalis, Moirans, France.

Time Delay Integration



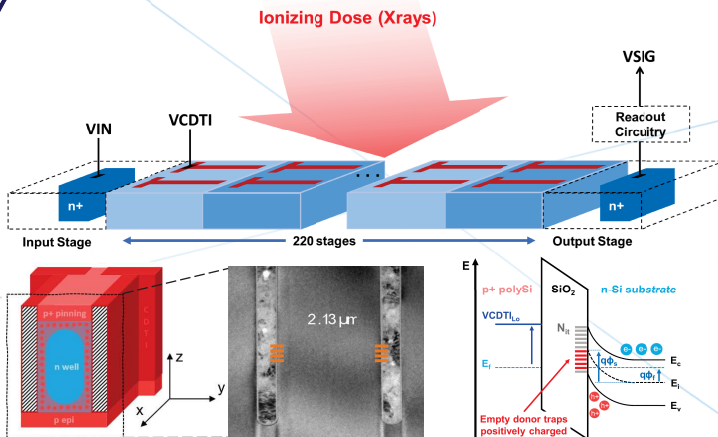
Space imaging is a very demanding field of activity requiring continuous technology improvements. CMOS Image Sensors (CIS), benefiting from constant advances on manufacturing process, naturally imposed themselves as the technology of choice to fulfill any space mission specifications. CIS thus supplanted Charge Coupled Devices (CCDs) offering a higher level of integration with on-chip CMOS functions, lower power voltage and improvements on radiation hardness by design. However CCD sensors still prove being perfectly fitted for High Resolution Earth scanning imaging applications using for instance Time Delay Integration (TDI). This imaging method capitalizes on the sensor's noiseless charge transfer feature by performing a simultaneous summation of charges with landscape scroll, allowing an artificial increase of exposure.

Device architecture



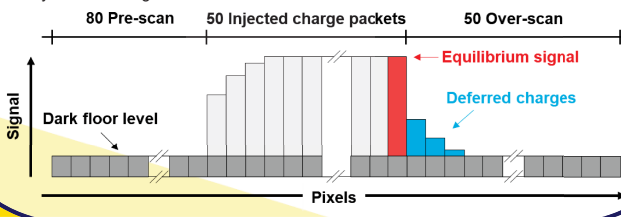
To take advantage of both CCD and CMOS technologies, Tourn et al. developed with STMicroelectronics a new kind of CCD manufactured in CMOS technology with Capacitive Deep Trench Isolation (CDTI) used as gates to shape vertically the potential of a n-type buried channel [1]. The resulting potential shape in between the two CDTI (axis x) is a parabola with a maximum found at W/2 implying the attraction of free charges to the center of the channel. The width W is reduced at the beginning of a phase to close the finger with a potential barrier by use of Transverse CDTI (TCDTI) with respect to the transfer direction. Consequently, integration is made possible while keeping all phases inverted at Low state and every interfaces passivated by a hole layer. This feature is known as Multi-Pinned Phase (MPP) [2]. Charge transfer is obtained by applying a positive voltage (High State) to the CDTI gates of the following phase. The existing TCDTI barrier is lowered under the floor of the first phase to allow charges to flow thanks to potential and charge concentration gradient.

Experimental Setup



It is well known that Total Ionizing Dose (TID) induces traps in oxides, dark current and Charge Transfer Inefficiency (CTI) increase in planar CCDs [3]. However it has never been evaluated on a trench based CCD of this kind. Electrical tests are performed on a single 220 pixels line register binned to an injection node and a sense node. Irradiation is performed with a tungsten tube X-ray set to deliver a TID of 10krad(SiO₂) in 10min and 100krad(SiO₂) after 1h40. TID effects are compared using dark current and Charge Transfer Inefficiency (CTI) measurements :

- Dark current measurement consists in determining the total signal dumped into the sense node with no illumination and a closed injection gate divided by the total integration time.
- CTI is measured using the Extended Pixel Edge Response method (EPER). 50 equal charge packets are injected into an empty register and transferred to the output node. Following these 50 pulses, some electrons that have been delayed due to trapping and re-emission mechanisms are measured in the form of a trail. Those are called "deferred charges" and helps determining the register ability to transfer signal.

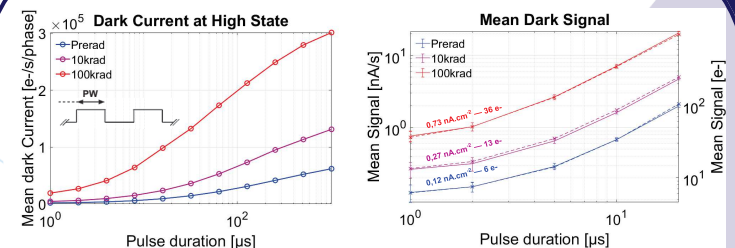


References

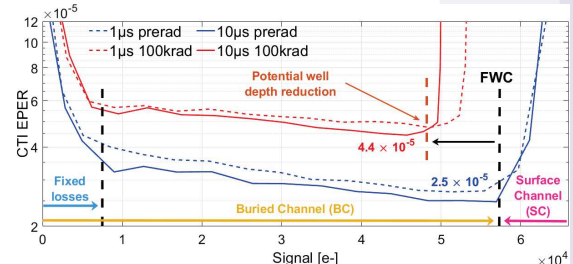
- P. Tourn, F. Roy, P. Magnan, O. Marcelot, S. Demiguel, et C. Vimontois, "Capacitive Trench-Based Charge Transfer Device", IEEE Electron Device Letters, vol. 41, n. 9, p. 1388-1391, sept. 2020.
- J. R. Janesick, T. Elliott, S. Collins, M. M. Blouke, et J. Freeman, « Scientific Charge-Coupled Devices », OE, vol. 26, n° 6, p. 692-714, août 1987.
- G. R. Hopkinson, "Radiation-induced dark current increases in CCDs", in RADECS 93. Second European Conference on Radiation and its Effects on Components and Systems, sept. 1993, p. 401-408.
- B. E. Burke et S. A. Gajar, "Dynamic suppression of interface-state dark current in buried-channel CCDs", IEEE Transactions on Electron Devices, vol. 38, n. 2, p. 285-290, févr. 1991.

Acknowledgement : The authors gratefully acknowledge CNES and Thales Alenia Space for co-funding this research. Useful discussion with J. Michelot from Pyxalis have been also appreciated to consolidate this work.

Results



The main asset of this CCD-on-CMOS device is the interface inversion property at Low State enabling holes to fill traps, hence mitigating dark current. Thanks to MPP operation, the High State duration when passivation is lost can be reduced in regards of the full cycle. It was found that the dark current rate is effectively quenched for transfer pulse shorter than the time constant associated to thermally generated charges. This feature is called Dynamic dark suppression [4]. As a result, the mean dark current in operational conditions is optimized for short transfer pulses (passivated at 85%).



One must insure of the proper capacity of the device to operate charge transfer for short phase aperture time. As a general trend, fixed losses are observed for low injections before CTI sets into proportional losses which translates into a plateau. At around 60ke- charge transfer transits from a buried storage regime to a surface storage regime promoting charge loss by surface trapping.

The surface trap density increase is the reason for more charges being delayed by the trap capture-release mechanisms. Additionally, TID induces a change in flatband voltage. As a result, the switch to surface regime occurs sooner and a diminution of the saturation level is observed as TID increases. Some well depth can be retrieved by lowering the gate voltage.

Overall, for a pulse width of 1μs no significant CTI degradation is observed proving the charge packet is fully transferred during this lap of time.