Analysis of the Single-Event Latch-up Cross Section of a 16nm FinFET System-on-Chip using Backside Single-Photon Absorption Laser Testing and Correlation with Heavy Ion Data

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Abstract

The SEL cross section of a 16nm finFET System on Chip (SoC) is investigated by combining Single Photon Absorption (SPA) laser testing, emission microscopy and embedded instrumentation. Results indicate the origin of latch-ups and present excellent correlation with heavy ion data.

Acknowledgement

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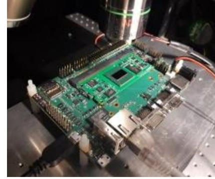
Introduction

- **Single-event latch-up:** a major concern in finFET technologies, observed in 16nm [1, 3, 4] and 7nm devices [2]
- SPA laser testing: an interesting complementary technique to spatially locate the origin of SEL events within a device
- Localization of SEL sensitivity in a 16nm finFET complex SoC?

Test bench and methodology

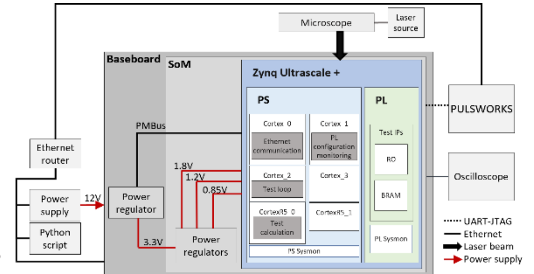
- Device under test:
  - Xilinx Zynq Ultrascale+ (XCZU3EG)
  - Technology: TSMC **16nm bulk finFET**
- Laser tests: **SPA laser system** @ IES Preserve
  - Wavelength: 1064nm
  - Pulse duration: 30ps
  - Spot size: 1.1µm

DUT under laser microscope



Simple HW setup complemented by embedded SW & IPs for self-testing with improved observability

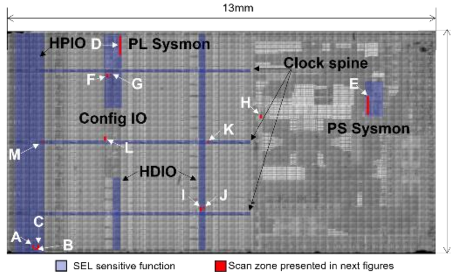
Experimental setup – hardware & software testbench



- Monitoring of the power supply currents
  - Externally at the level of the base-board 12V supply
  - Lower voltages SoM power lines not monitored individually

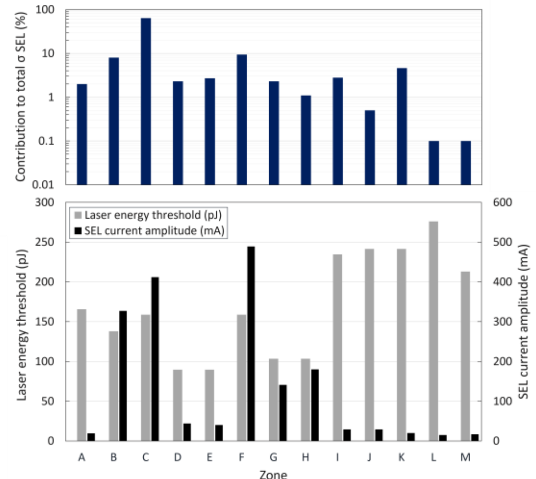
Experimental results

SEL sensitive regions overview



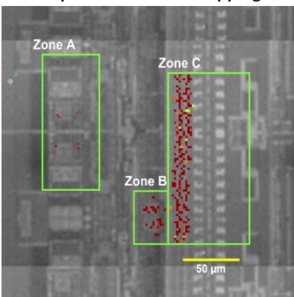
- **SEL mappings** performed on the different sensitive regions to extract:
  - Laser **energy threshold**
  - SEL **sensitive area** as a function of the laser energy
- Most of SEL-sensitive areas are located in the **Programmable Logic (PL)**

Details on SEL sensitive area

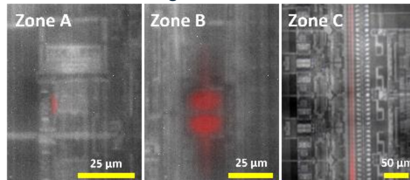


- **Main contributors** to the total SEL cross section:
  - Structures related to HPIO banks
- Highest SEL current observed in zone F
- Several small zones with higher energy threshold (I to M)
- Lowest energy threshold: **PL & PS Sysmon units** (D, E)

Examples of SEL laser mappings



SEL-induced light emission observation



- Zones A, B and C repeated over the full width of the chip
- **EMMI images** associated to SEL triggering confirm the latch-up nature of the events

Correlation & Discussion

Correlation with heavy ion data

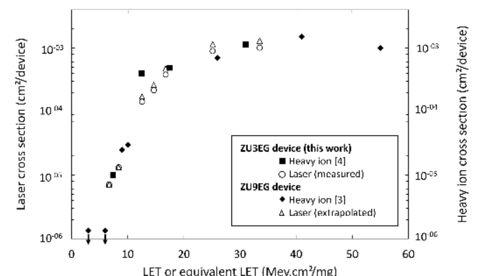
- Heavy ion data from [3, 4]
- **Equivalent LET** of each laser pulse energy is calculated with [5]: $LET_{laser} = \frac{E_{pair}}{d_V} \iiint_V N_{laser}(r)dr$
- Laser results for the ZU3EG extrapolated to the ZU9EG device by considering the number of banks

Good correlation between laser and heavy ion data both for the threshold LET and the saturation cross section

Discussion

- No significant contribution to the SEL cross section missed during our tests
- No SEL triggered in the core-logic of both the PS and the PL
  - SEL in this SoC probably only occurs in **mixed-signal and IO circuits** connected to the **1.8V or 1.2V supplies**

SEL cross section – Laser / heavy ion correlation



Conclusions

- Analysis of the SEL cross section of a complex programmable SoC
- Simple electrical setup + DUT-embedded instrumentation, SPA laser testing + in-line light emission microscopy
- SEL sensitive areas and functions identified
- Good correlation of laser testing results with heavy ion data
- No SEL is triggered in the core-logic sections of this device
- IOs are the main contributors to the SEL cross section at high LET

References

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[5] V. Pouget et al, "Theoretical Investigation of an Equivalent Laser LET," Micro. Rel., vol. 41, 2001.