Design of a new readout circuit for a highly dense hybrid detector

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CONTEXT

What do we want to understand ?

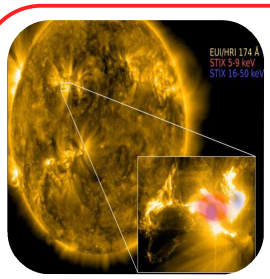


Fig 1: Sun in EUV view (solar flare focus)

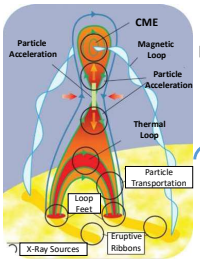


Fig 2: Schematic representation Of a solar eruptive event

What do we need:

- Localizing and measuring Energy of X-ray photons **0.5-100 keV** With:

High spectral resolution to study thermal and non-thermal emission mechanisms.

High spatial resolution to discriminate different X-ray generating events.

Sun and its Magnetic Field

How to measure ?

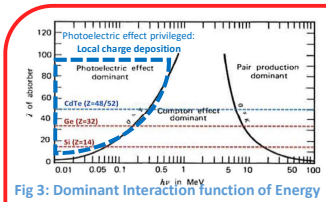


Fig 3: Dominant Interaction function of Energy and Atomic Number Z

Aimed spectral resolution: **500 eV @ 60 keV (FWHM)**

Low noise (< 20 el.rms)

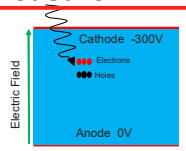


Fig 4: Photoelectric interaction in Detector

Low noise (< 20 el.rms)

Low leakage current (~1pA)

Low capacitance (~300 fF)

Schottky contact

Operating at – 20 °C

CdTe based Semiconductor Detector (1000 µm thick)

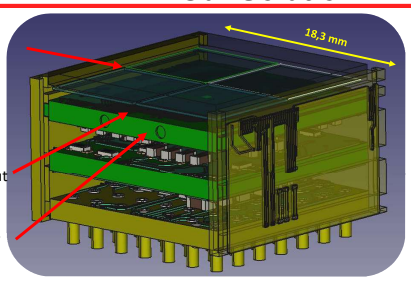
Detection Principle : Photoelectric Effect

Our Solution

CdTe pixel detector (64x64 pixels 250 µm pitch)

4 Full-Custom front-end Pixelated Readout ASIC

3D Packaging (full-custom ADC "OWB-1")



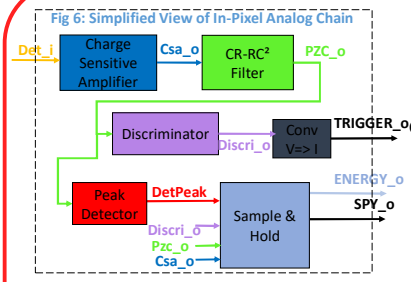
- **Maximum pixel size** : 250 μm x 250 μm
- **Energy Range** = 1 – 220 keV
- **1st fully digital single photon counting module**
- 32 channels full-custom ADC

Fig 5: Mini CdTe On-Chip (MC2 Module)

4 Sides Abutable, Compact, and fully digital Imaging Spectroscopy Module

My work

Fig 6: Simplified View of In-Pixel Analog Chain



High Spectral Resolution Readout ASIC

High Spectral Resolution needs Low noise Analog Channel

Charge Sensitive Amplifier has the most important impact on the noise

Design a Proto-Chip to test and study different optimizations and architectures for CSA

Design prototype ASIC (Application Specific Integrated Circuit)

DESIGN

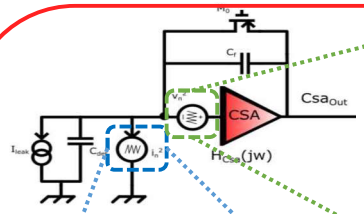


Fig 7:Charge Sensitive Amplifier Noise Model

contribution of input noise considered as a voltage noise

Mainly Determined by the **Voltage Amplifier's Input Transistor**

Thermal Noise (agitation of charge carriers)

Flicker Noise (MOS fabrication process)

contribution of input noise considered as a current

Mainly Determined by the **Detector** and the **Reset Transistor**

Shot Noise (discrete nature of electric current)

Parallel Thermal Noise (agitation of Reset MOS charge carriers)

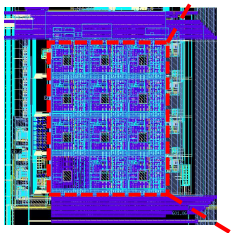


Fig 8: Close-up look on the ChipTest

$$ENC = \sqrt{ENC_{//}^2 + ENC_{Th}^2 + ENC_{1/f}^2}$$

Charge Sensitive Amplifier Noise Model

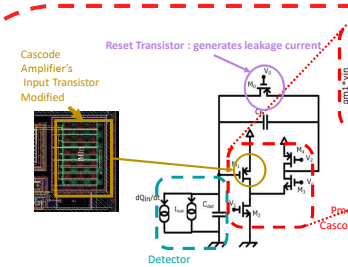


Fig 9: Pmos based Charge Sensitive Amplifier Circuit

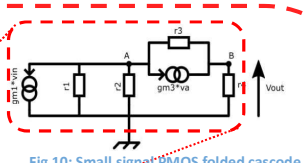


Fig 10: Small signal PMOS folded cascode

We need A_0 to be high:
A_0 *Cr>> Cdet

$$A_0 = \frac{gm_1 r_4}{1 + \frac{(r_3+r_4)}{r_1 r_2 \cdot (1+gm_3 r_3)}}$$

$$A_0 \simeq gm_1 r_4$$

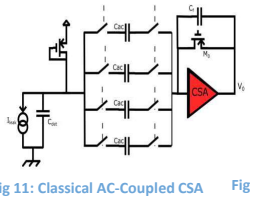


Fig 11: Classical AC-Coupled CSA (Cac ={0.1; 1 ;10; 30 pF}

Require High Value Capacitance to maintain Gain

Cac min =30 pF (inconceivable)

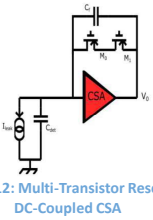
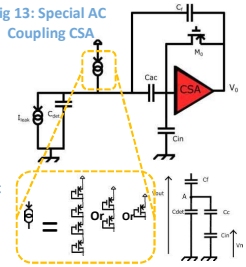


Fig 12: Multi-Transistor Reset DC-Coupled CSA

Dynamic Range Collapse with Two Reset Transistors

Fig 13: Special AC Coupling CSA



Mini Matrix of Pixels with Different Charge Sensitive Amplifier Architectures

RESULTS

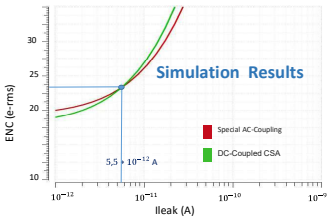


Fig 14: Equivalent Noise Charge Function Leakage Current

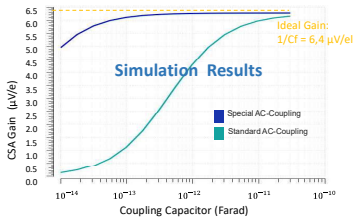


Fig 15: AC Classic VS AC Special Function Coupling Capacitor

PERSPECTIVES

Total Ionizing Dose (TID) on X-FAB Technology

- Gamma Rays : 100 Krad / 1Mrad
- **"Cocase"** component irradiation bench ^{60}Co. (CEA)

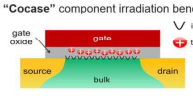


Fig 16: Dose effect on MOSFET (side view)

P-MOSFETs
1. Trapped holes: + Vth ↓
2. Interface traps: + Vth ↓ Leakage Current ↑

N-MOSFETs
1. Trapped holes: + Vth ↓
2. Interface traps: + Vth ↑ Leakage Current ↑

PhD Perspective:

- **Reception of ASIC**
- **Wire Bonding**
- **Characterization Of Pixels: Validation of Noise Calculation Models for the New architectures (<20 el.rms Expected).**
- **Choosing the most performing pixel for MC2**

MC2 Project:

- **Design of a full scale Readout ASIC (32x32 or 48x48 pixels) with the pixel architecture chosen from my work.**