Efficient designs of on-board heterogeneous embedded systems for space applications

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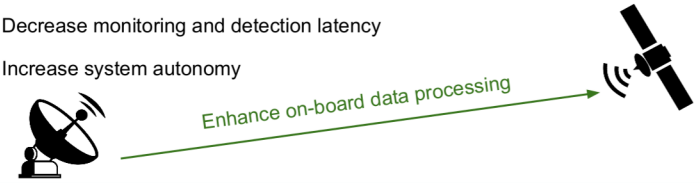
Abstract

- On-board payload data processing on space-qualified heterogeneous Multiprocessor System-on-Chip (MPSoC)
- Design space exploration by combining the roofline model with High-Level Synthesis (HLS) for hardware accelerator architecture design

Introduction

- Decrease monitoring and detection latency
- Increase system autonomy



Design Space Exploration (DSE) methodology

Roofline performance model

- Computational ceiling and Input/Output (I/O) bandwidth ceiling
- Implementation can be memory-bound or compute-bound.

High-Level Synthesis (HLS)-based hardware accelerators

- Generation of different Field-Programmable Gate Array (FPGA) accelerator designs faster and easier
- Refactorization of initial C/C++ codes using pragmas and directives

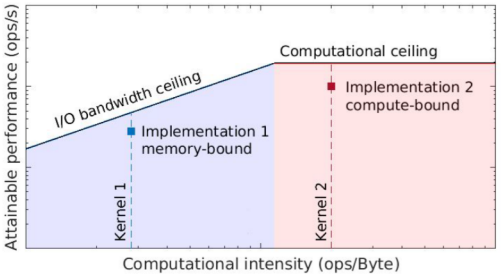


Fig. 1 Roofline performance model [1]

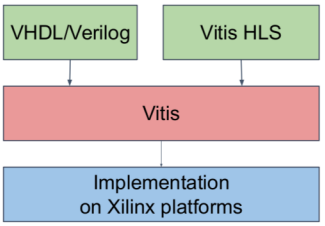


Fig. 2 Development flow of Xilinx FPGA hardware accelerators

DSE use-case: 2-Dimensional Fast Fourier Transform (2-D FFT)

2-D FFT

- Study case: SVOM ECLAIRs coded-mask telescope [2]

Table. 1 Prioritized algorithms from the survey with payload teams

Classification	Sub-classification	Number of users
Fourier transform	FFT, IFFT, DFT	5
Filter	IIR, CIC	4
	Kalman	1
Compression	CCSDS 121-124	3
Optimization	Interpolation	2
	Fitting and correlation	2
	Gradient descent	2
Histogram		1
Digital Elevation Model		1

Heterogeneous embedded system including an FPGA

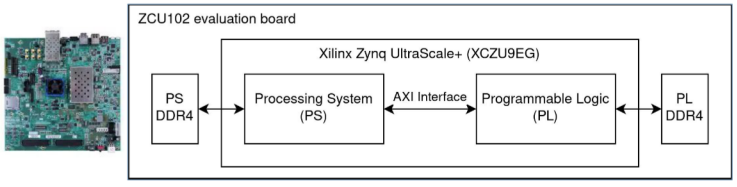


Fig. 3 Xilinx Zynq UltraScale+ evaluation board (ZCU102)

HLS-based 2-D FFT hardware accelerator design

- Xilinx Vitis HLS-based 2-D FFT library with high parallelism and pipelining
- Loop pipelining modification considering the hardware resources

FPGA Roofline model

- Computational ceiling: Digital Signal Processing (DSP) slices and clock frequency
- I/O bandwidth ceiling: Advanced eXtensible Interface (AXI) and DDR4 memory

Theoretical FPGA roofline model targeting the Zynq UltraScale+ platform

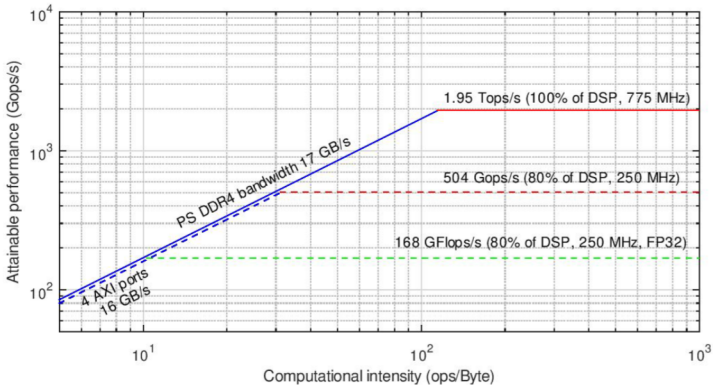


Fig. 4 Theoretical FPGA Roofline model of ZCU102 based on DSP slices

Application-specific FPGA roofline model with accelerator designs

- Execution time < 5 ms, memory-bound kernel

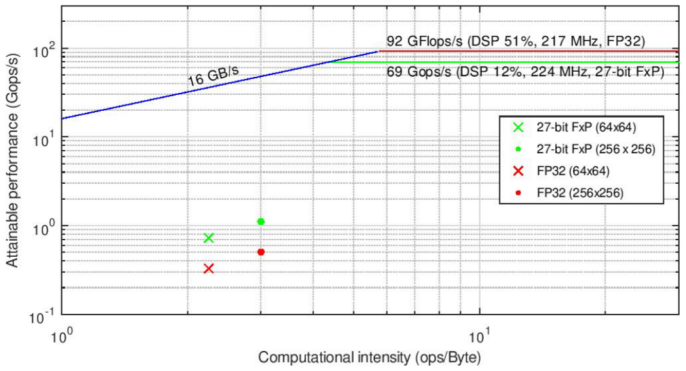


Fig. 5 FPGA Roofline model of ZCU102 for 2-D FFT based on DSP slices

Conclusion

- Possibility of migrating payload data processing pipelines to on-board embedded systems
- Combination of the roofline model with HLS-based DSE for effective performance analysis and architectural exploration

References

[1] S. Williams, A. Waterman, and D. Patterson, “Roofline: an insightful visual performance model for multicore architectures,” Commun. ACM, vol. 52, no. 4, pp. 65–76, Apr. 2009

[2] S. Schanne et al., “A Scientific Trigger Unit for space-based real time gamma ray burst detection I - Scientific software model and simulations,” IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC), Oct. 2013, pp. 1–5

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