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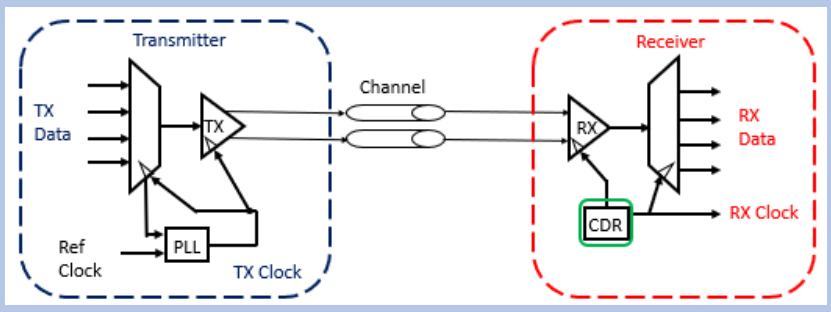
# Réalisation et optimisaton d'une horloge à récupération de données pour lien à très haut débit par verrouillage à injection d'oscillateurs en anneaux et ciblant des technologies nanométriques

## Introduction

- To support increasing data rates => New solutions for high speed data link are investigated.
- Clean frequency synthesizers require low phase noise, low power consumption and the lowest locking time.

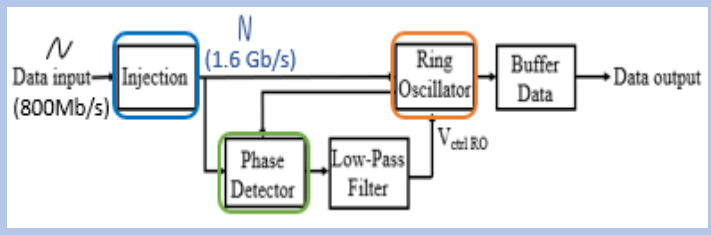



SerDes Architecture

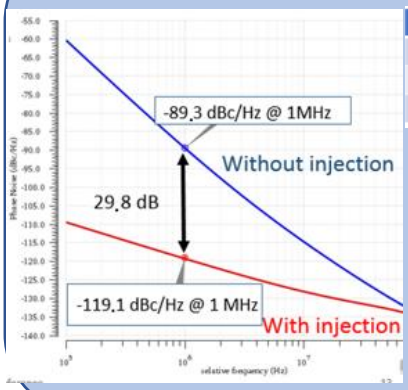
- SerDes commonly used in wireline high speed communication systems.
- Serialization of the data from TX, sent through channels to the RX part.
- RX recovers the correct data streams thanks to the **CDR** block.

## Overall circuit architecture

- Injection block => Injection locking
- Ring Oscillator => Frequency generation
- Phase Detector => Phase comparison




## Result simulations




| | RO w/o injection | PLL w/ injection |
|---|---|---|
| PN @ 1 MHz | -89.3 dBc/Hz | -119.1 dBc/Hz |
| Jitter | 35 mUI | 0.6 mUI |
| Eye Opening | 467 mUI/412 mV | 499 mUI/239 mV |

| | This work ** | [3] | [17] | [18] |
|---|---|---|---|---|
| Process/Supply Voltage | 180nm/1.8V | 180nm/1.8V | 180nm/1.8V | 180nm/1.8V |
| Power dissipation (mW) | 41* | 174 | 18.4 | 62 |
| Bit rate (Gbits/s) | 1.6 | 10 | 0.4-2.4 | 0.32-2.7 |
| Phase Noise at 1 MHz(dBc/Hz) | -119.1 | - | - | -97.6** |
| Jitter (mUI) | 0.6 | 3.6 | 10.8 | 159 |
| Locking time (µs) | 0.02 | 200 | - | 15.2 |
| Core area ($mm^2$) | 0.10 | 1.96 | - | - |

## Conclusion

- PN, jitter & locking time improved due to Injection locking.
- Improvements ? Cut off injection locking to reduce power consumption.

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